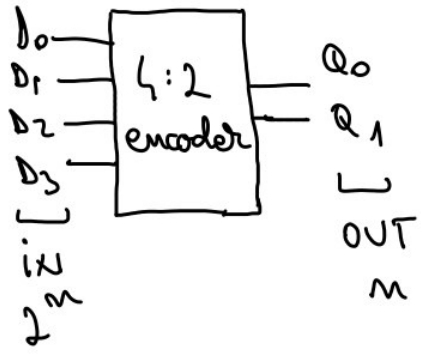
Seminar nr. 5.

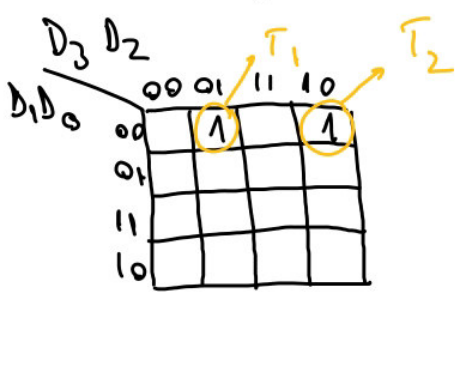
Codificator binar (codificator de adresă)
("binary encoder")

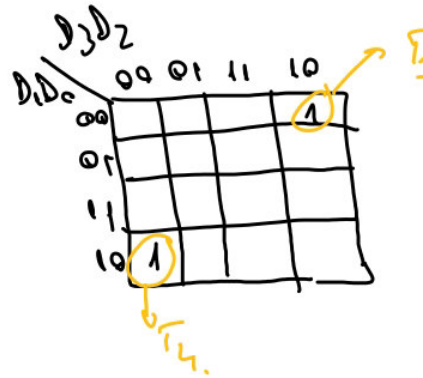
encoder 4:2



D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

$Q_1 = T_1 + T_2$ $\qquad$ $Q_0 = \bar{T}_3 + T_4$





$$SOP: Q_1 = \bar{D}_3 D_2 \bar{D}_1 \bar{D}_0 + D_3 \bar{D}_2 \bar{D}_1 \bar{D}_0 =$$

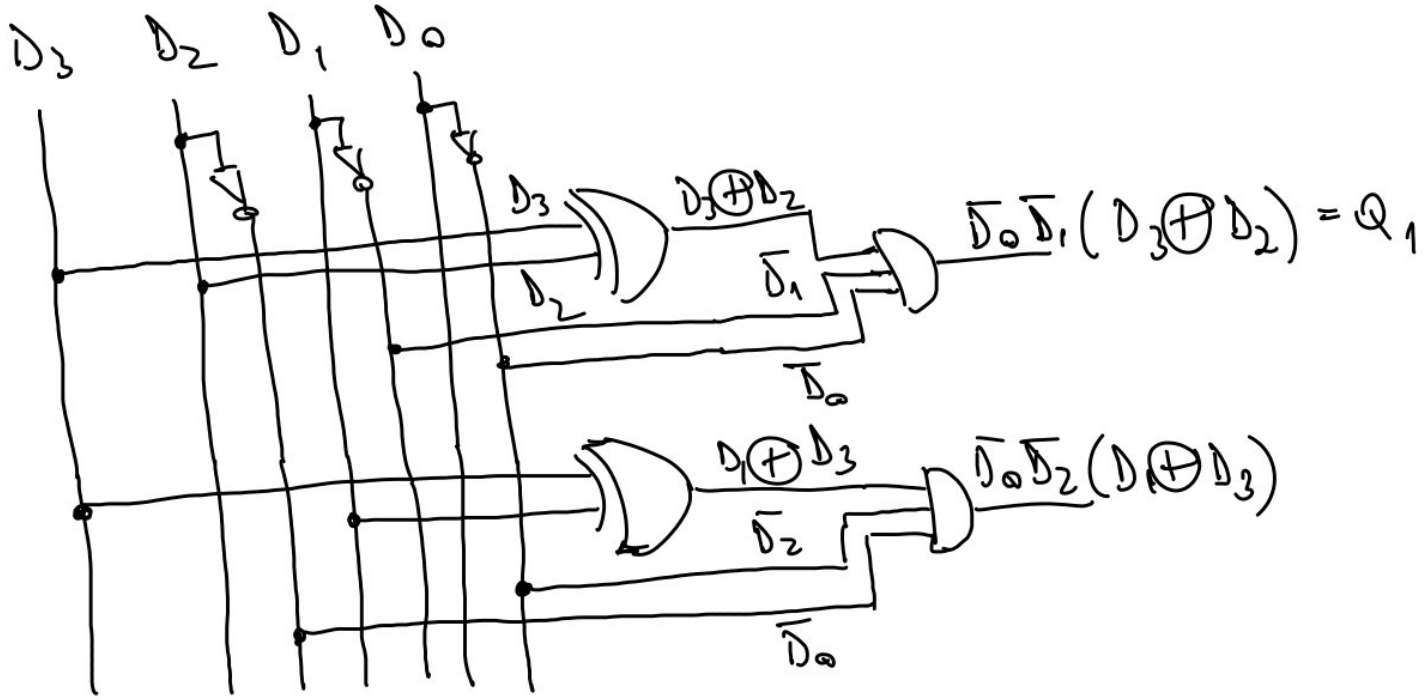
$$= \bar{D}_1 \bar{D}_0 (\bar{D}_3 D_2 + D_3 \bar{D}_2) = \bar{D}_1 \bar{D}_0 (D_3 \oplus D_2)$$

$$\left(A \oplus B = A\bar{B} + \bar{A}B \right)$$

$$\overline{A \oplus B} = AB + \bar{A}\bar{B}$$

$$Q_0 = \bar{D}_3 \bar{D}_2 D_1 \bar{D}_0 + D_3 \bar{D}_2 \bar{D}_1 \bar{D}_0 =$$

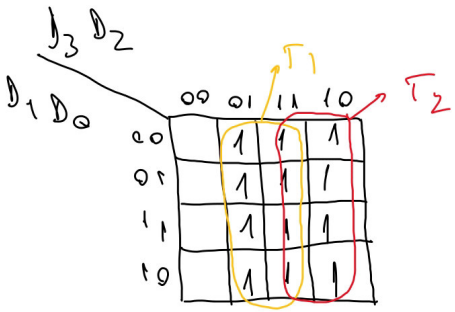
$$= \bar{D}_0 \bar{D}_2 (\bar{D}_3 D_1 + D_3 \bar{D}_1) = \bar{D}_0 \bar{D}_2 (D_1 \oplus D_3)$$

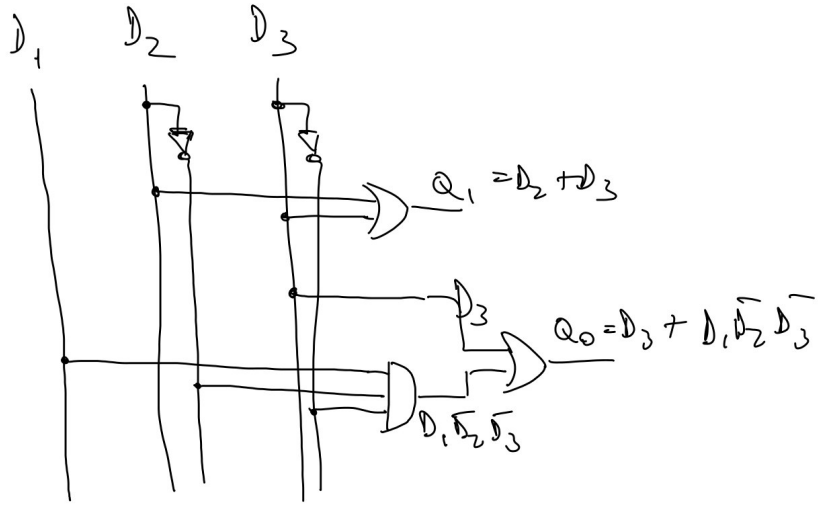


Priority encoder :

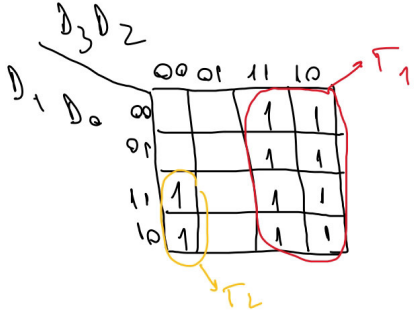
D_3	D_2	D_1	D_0	Q_1 Q_0
0	0	0	1	0 0
0	0	1	X	0 1
0	1	X	X	1 0
1	X	X	X	1 1

$$Q_1 = D_2 + D_3$$





$$Q_0 = D_3 + D_1 \bar{D}_2 \bar{D}_3$$

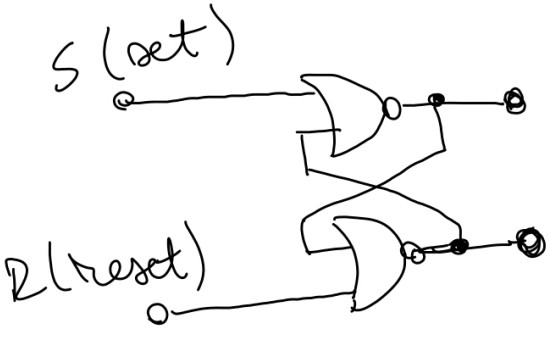


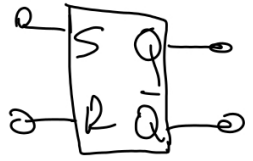
Circuite logice secvențiale:

- starea ieșirilor depinde atât de starea intrărilor cât și de stările precedente de la ieșire.

→ memorie.

Circuitul basculant bistabil RS:

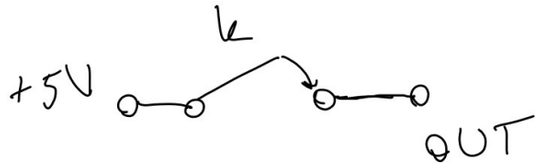




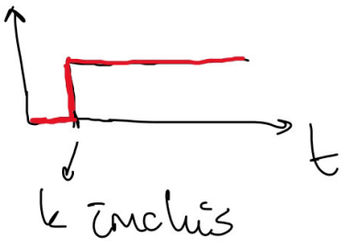
Q_n - starea actuală
Q_{n-1} - starea precedentă

S	R	Q_n	$\bar{Q}_n$	
0	0	Q_{n-1}	$\bar{Q}_{n-1}$	(no change) latch.
0	1	0	1	reset
1	0	1	0	set
1	1	?	?	→ undefined (illegal state)

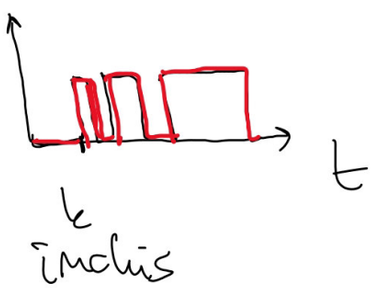
switch debouncing.



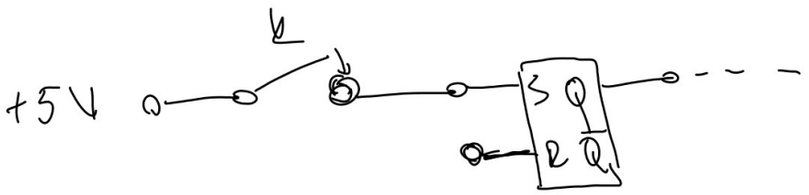
ideal

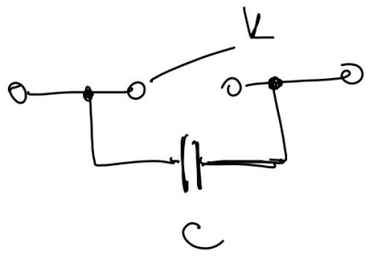


real

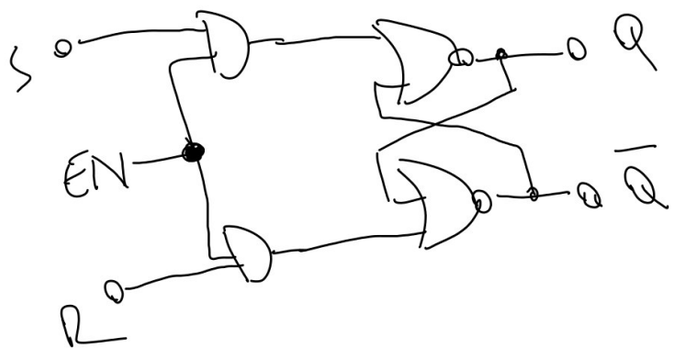


soluția:



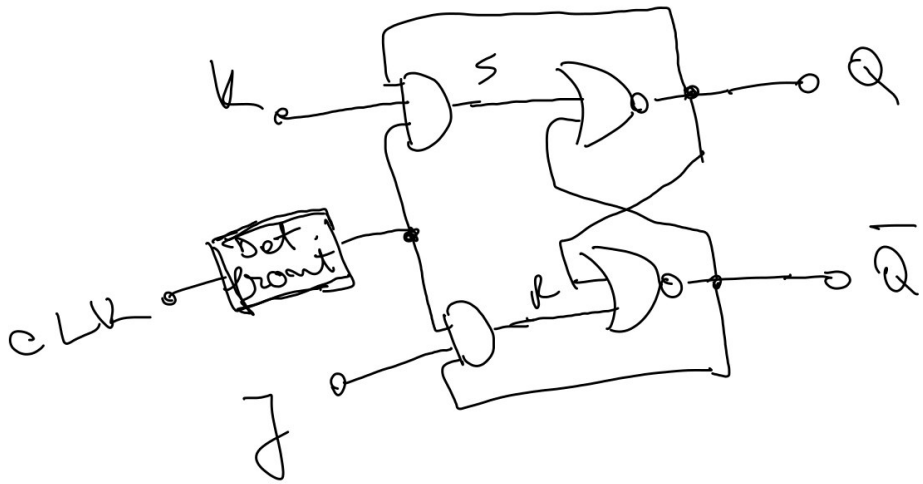


CBB RS cu poartă („gated RS")



EN	S	R	Q_M	$\overline{Q_M}$	
1	0	0	Q_{M-1}	$\overline{Q_{M-1}}$	
1	0	1	0	1	
1	1	0	1	0	
1	1	1	?	?	
0	0	0	Q_{M-1}	Q_{M-1}	(latch
0	0	1	latch		
0	1	0	latch		
0	1	1	latch		

CBB Jk (Jam-keep / Jack Kilby).



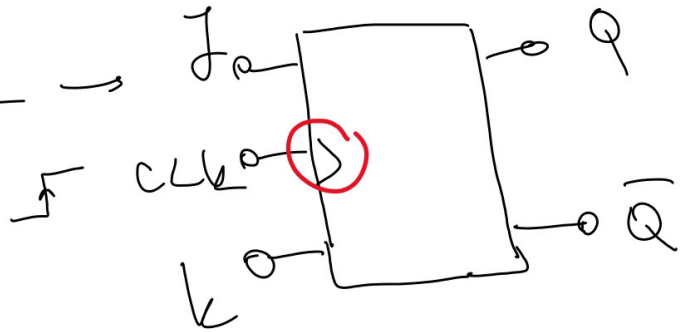
front crescător

„rising edge"

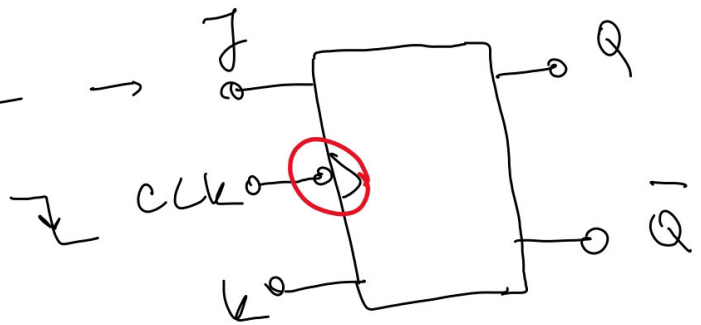
front descrescător

„falling edge".

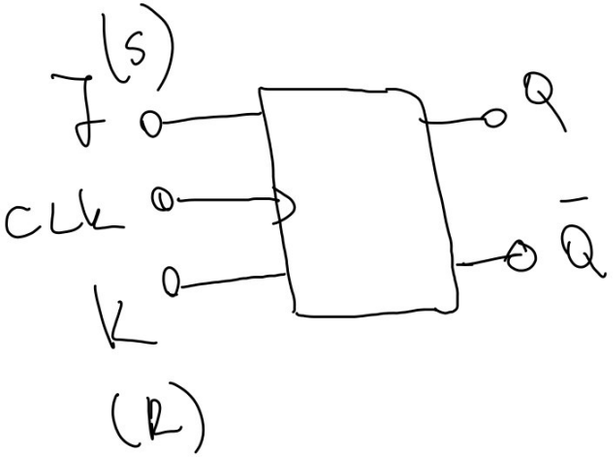
rising edge Jk →



falling edge Jk →

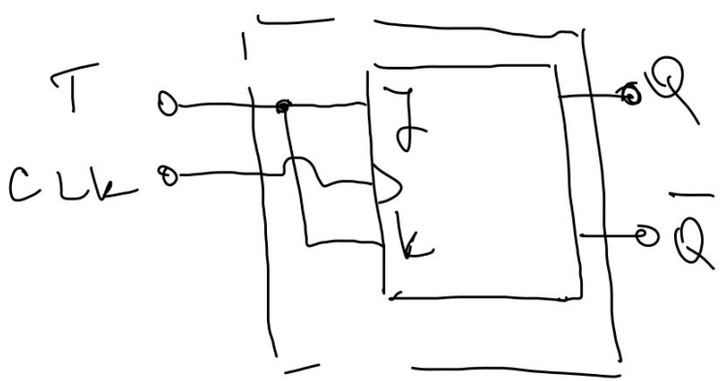


Tabelul de adevăr pentru un CBB JK cu front descător.



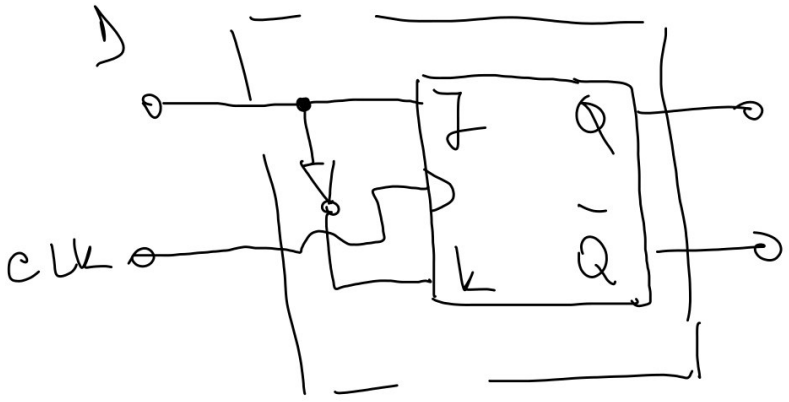
CLK	J	K	Q_n $\bar{Q}_n$	
↓	0	0	Q_{n-1} $\bar{Q}_{n-1}$	latch
↓	0	1	0 1	keep (reset)
↓	1	0	1 0	jam (set)
↓	1	1	$\bar{Q}_{n-1}$ Q_{n-1}	toggle
x	0	0	latch	
x	0	1	latch	
x	1	0	latch	
x	1	1	latch	

Bistabilul „T" (toggle):



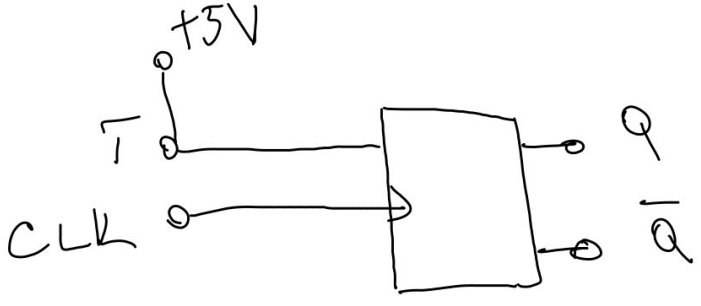
CLK	T	Q_n $\bar{Q}_n$	
↓	0	Q_{n-1} $\bar{Q}_{n-1}$	latch
↓	1	$\bar{Q}_{n-1}$ Q_{n-1}	toggle
x	0	latch	
x	1	latch.	

Bistabilul „D" (data):

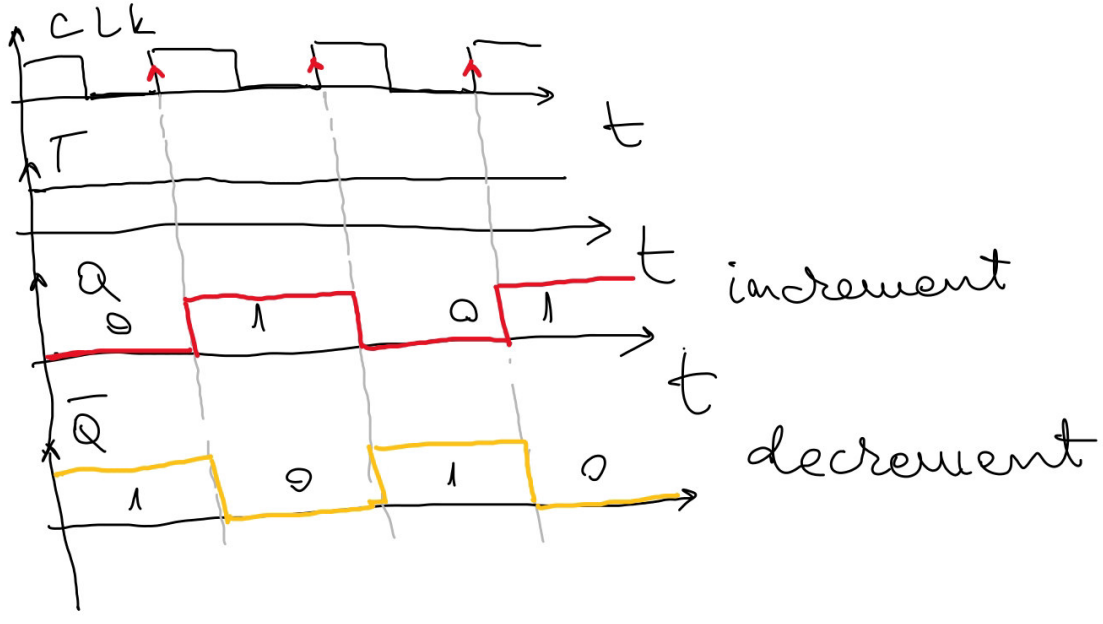


CLK	D	Q_n	$\bar{Q}_n$
↑	0	0	1
↓	1	1	0
X	0	latch	
X	1	latch	

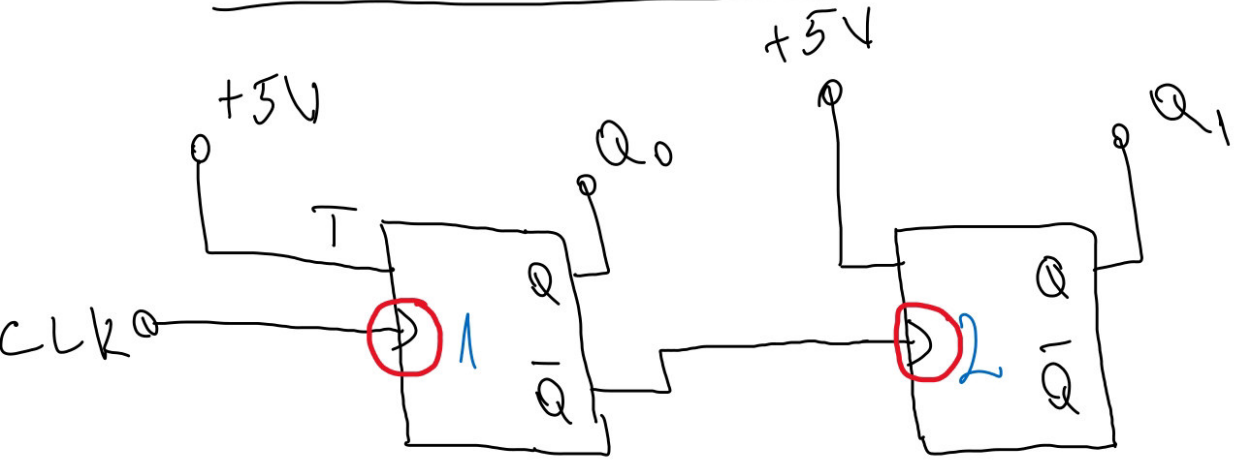
Numărător MOD-2 cu CBB T:



Presupunem Q=0 la t=0



Numărător asincron MOD-4:



CLK	Q_1 (MSB)	Q_0 (LSB)
0	0	0
1	0	1
2	1	0
3	1	1